// VerilogA for ADC\_Ideal\_4bit\_FlashADC, VerilogA\_LadderAndComparators, veriloga

`include "constants.vams"

`include "disciplines.vams"

module VerilogA\_LadderAndComparators(vin,clk,vmax,vmin,t0,t1,t2,t3,t4,t5,t6,t7,t8,t9,t10,t11,t12,t13,t14);

parameter real vtrans=0.5;

parameter real delay = 0;

parameter real ttime = 1p;

parameter real clk\_threshold = 0.9; //vdd is 1.8v

input clk,vin,vmin,vmax;

output t0,t1,t2,t3,t4,t5,t6,t7,t8,t9,t10,t11,t12,t13,t14;

electrical vin,vmin,vmax,clk;

electrical t0,t1,t2,t3,t4,t5,t6,t7,t8,t9,t10,t11,t12,t13,t14;

real step;

real t\_0,t\_1,t\_2,t\_3,t\_4,t\_5,t\_6,t\_7,t\_8,t\_9,t\_10,t\_11,t\_12,t\_13,t\_14;

analog begin

step = (V(vmax)-V(vmin))/16;

// Sampling Phase (-1 is for falling edge)

@(cross(V(clk) - clk\_threshold, -1))

begin

if (V(vin) > step+V(vmin)) begin

t\_0 = 1;

end

else begin

t\_0 = 0;

end

if (V(vin) > ((2\*step)+V(vmin))) begin

t\_1 = 1;

end

else begin

t\_1 = 0;

end

if (V(vin) > ((3\*step)+V(vmin))) begin

t\_2 = 1;

end

else begin

t\_2 = 0;

end

if (V(vin) > ((4\*step)+V(vmin))) begin

t\_3 = 1;

end

else begin

t\_3 = 0;

end

if (V(vin) > ((5\*step)+V(vmin))) begin

t\_4 = 1;

end

else begin

t\_4 = 0;

end

if (V(vin) > ((6\*step)+V(vmin))) begin

t\_5 = 1;

end

else begin

t\_5 = 0;

end

if (V(vin) > ((7\*step)+V(vmin))) begin

t\_6 = 1;

end

else begin

t\_6 = 0;

end

if (V(vin) > ((8\*step)+V(vmin))) begin

t\_7 = 1;

end

else begin

t\_7 = 0;

end

if (V(vin) > ((9\*step)+V(vmin))) begin

t\_8 = 1;

end

else begin

t\_8 = 0;

end

if (V(vin) > ((10\*step)+V(vmin))) begin

t\_9 = 1;

end

else begin

t\_9 = 0;

end

if (V(vin) > ((11\*step)+V(vmin))) begin

t\_10 = 1;

end

else begin

t\_10 = 0;

end

if (V(vin) > ((12\*step)+V(vmin))) begin

t\_11 = 1;

end

else begin

t\_11 = 0;

end

if (V(vin) > ((13\*step)+V(vmin))) begin

t\_12 = 1;

end

else begin

t\_12 = 0;

end

if (V(vin) > ((14\*step)+V(vmin))) begin

t\_13 = 1;

end

else begin

t\_13 = 0;

end

if (V(vin) > ((15\*step)+V(vmin))) begin

t\_14 = 1;

end

else begin

t\_14 = 0;

end

end

@(cross(V(clk) - clk\_threshold, +1))

begin

t\_0 = 0;

t\_1 = 0;

t\_2 = 0;

t\_3 = 0;

t\_4 = 0;

t\_5 = 0;

t\_6 = 0;

t\_7 = 0;

t\_8 = 0;

t\_9 = 0;

t\_10 = 0;

t\_11 = 0;

t\_12 = 0;

t\_13 = 0;

t\_14 = 0;

end

V(t0) <+ transition(t\_0,delay,ttime);

V(t1) <+ transition(t\_1,delay,ttime);

V(t2) <+ transition(t\_2,delay,ttime);

V(t3) <+ transition(t\_3,delay,ttime);

V(t4) <+ transition(t\_4,delay,ttime);

V(t5) <+ transition(t\_5,delay,ttime);

V(t6) <+ transition(t\_6,delay,ttime);

V(t7) <+ transition(t\_7,delay,ttime);

V(t8) <+ transition(t\_8,delay,ttime);

V(t9) <+ transition(t\_9,delay,ttime);

V(t10) <+ transition(t\_10,delay,ttime);

V(t11) <+ transition(t\_11,delay,ttime);

V(t12) <+ transition(t\_12,delay,ttime);

V(t13) <+ transition(t\_13,delay,ttime);

V(t14) <+ transition(t\_14,delay,ttime);

end

endmodule